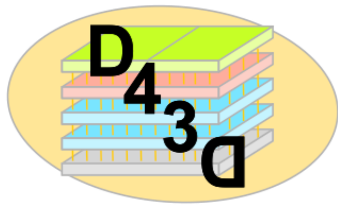

# D43D Workshop, June 23rd & 24th, 2014
# EPFL, School of Computer and Communication Sciences (IC)

**WiFi:** Username: x-d43d Password: taddam37 (6 char. + 2 digits)

## Day 1: Monday, June 23rd, 2014

| | | |
|---|---|---|
| 08:45-09:00 | Welcome / Badge Pickup | |
| 09:00-09:15 | Opening | Pascal Vivet, CEA-LETI |
| 09:15-10:00 | **Keynote: 3D Packaging Technologies and Industry Trends** | Thibault Buisson, Yole |
| 10:00-10:30 | COFFEE BREAK | |
| | **Session I - 3D Technology** **Chair: Patrick Leduc, CEA-LETI** | |
| 10:30-11:00 | 3D Technology for Power Efficient Computing | Patrick Leduc, CEA-LETI |
| 11:00-11:30 | Processor-WideIO Integration: Challenges and Solutions | Andy Heinig, Fraunhofer |
| 11:30-12:00 | RF characterization and modeling of TSV | Thierry Lacrevaz, University of Savoie |
| 12:00-13:30 | LUNCH @ Starling Hotel | |
| 13:30-14:00 | **Session II - 3D Computing Architectures** **Chair: Koji Inoue, Kyushu University** | |
| 13:30-14:00 | Heterogeneous Multi-core Processors using Through-Chip Wireless Interconnect | Hideharu Amano, Keio University |
| 14:00-14:30 | A Modular Shared L2 Memory Design for Three Dimensional Integration | Erfan Azarkhish, UNIBO |
| 14:30-15:00 | Using 3D Active Interposer for Scalable and Power Efficient Many-core Architectures | Denis Dutoit, CEA-LETI |
| 15:00-15:30 | Accelerating Big Data Services: It's All About Memory! | Babak Falsafi, EPFL |
| 15:30-16:00 | COFFEE BREAK | |
| | **Session III – 3D Thermal Effects** **Chair: Giovanni Ansaloni, EPFL** | |
| 16:00-16:30 | Integrated Cooling and Power Generation of 3D MPSoCs with Microfluidics | Mohamed Sabry, Stanford University |
| 16:30-17:00 | Orthogonal Scaling: The future path for denser and yet, more efficient systems | Arvind Sridhar, IBM Research |
| 17:00-17:30 | Thermal analysis and model identification techniques for a logic + WIDEIO stacked DRAM test chip | Andrea Bartolini, ETHZ |
| 17:30-18:00 | Thermal-Aware Automated Floorplaning for 3D MPSoCs | Jose L. Ayala, UCM |

## Day 2: Tuesday, June 24th, 2014

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|---|---|---|
| 08:30-08:45 | Opening | |
| 08:45-09:30 | **Keynote: 3D Processor: Are we ready yet?** | Yuan Xie, Pennsylvania State University |
| 09:30-10:00 | COFFEE BREAK | |
| | **Session IV - 3D Interconnects and Memories Chair: Christian Weis, UKL** | |
| 10:00-10:30 | DiRAM4, A Revolutionary 3D DRAM Architecture | Robert Patti, Tezzaron |
| 10:30-11:00 | 2.5D and 3D Integration of Ultra High Bandwidth Memories | Aaron Nygren, Micron |
| 11:00-11:30 | Thermal and Power Aspects of MPSoCs with WIDE I/O DRAMs | Matthias Jung, Univ. of Kaiserslautern |
| 11:30-12:00 | Accelerating In-Memory MapReduce with Near Data Processing | Rajeev Balasubramonian, Univ. of Utah & HP Labs |
| 12:00-13:30 | LUNCH @ Starling Hotel | |
| 13:30-14:00 | **Session V - 3D Testability and Reliability<br>Chair: Vasilis Pavlidis, Manchester University** | |
| 13:30-14:00 | Towards Design for 3D Reliability - Stack Package Interaction | Gerd Schlottig, IBM |
| 14:00-14:30 | Key Enablers for 3D/2.5D Integration - Material, Process and Reliability | Chuan Seng Tan, NTU |
| 14:30-15:00 | Imec's 3D-DfT Architecture: Basics, Extensions, and Demonstrator Results | Tobias Burgherr, IMEC |
| 15:00-15:30 | 2D to 3D Test Pattern Retargeting using IEEE P1687 based 3D DFT Architectures! | Yassine Fkih, LIRMM |
| 15:30-16:00 | COFFEE BREAK | |
| | **Session VI – 3D CAD Tools Chair: Pascal Vivet, CEA-LETI** | |
| 16:00-16:20 | Towards thermal-Aware Analysis and Debug of 3D-IC | Sylvian Kaiser, DOCEA Power |
| 16:20-16:40 | IP and SoC-level design co-optimization for efficient 3D-integration: methodologies and EDA tools and Standards | Ravi Varadarajan, Atrenta |
| 16:40-17:00 | 3D Flow for sign-off | Alexandre Arriordaz, Mentor Graphics |
| 17:00-17:20 | Which Design Methodology for Monolithic 3D Integration | Sebastien Thuriès, CEA-LETI |
| 17:20 | Closing | |