Designing Heterogeneous Chips With zGlue

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Outline

• Background
• zGlue Integration Platform (ZiP)
• zGlue ChipBuilder CAD
• How to Design with ChipBuilder
• Economics of Chiplets
• Q&A
Custom Chips on Demand
zGlue pitches 'chiplets' to make custom chips for startups

zGlue Aims to Make It Cheap and Easy to Produce Wearables and Other IoT Hardware

zGlue launches a configurable system-on-a-chip to help developers implement customized chipsets

Startup Debuts 2.5D Design Service
zGlue launches open beta of online tool
The Opportunity: 1,000X More Customized Devices
1. Customization
## 2. Time

**PRODUCT CYCLE** for Chip Development: An Example

<table>
<thead>
<tr>
<th>Design</th>
<th>Prototype</th>
<th>Evaluation</th>
<th>Mass Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>![Design Icon]</td>
<td>![Prototype Icon]</td>
<td>![Evaluation Icon]</td>
<td>![Mass Production Icon]</td>
</tr>
<tr>
<td><strong>6</strong> MONTHS</td>
<td><strong>3</strong> MONTHS</td>
<td><strong>1</strong> MONTH</td>
<td><strong>9</strong> MONTHs</td>
</tr>
</tbody>
</table>

**SoC**

- System-on-Chip

- **ZiP**
  - zGlue-Integration Platform

- **Time**
  - 10 hours
  - 1 month
  - 1 week
  - 3 months
3. Miniaturization
Iterate Hardware like Software
Streamlined Process to Empower Millions of Innovators

Design

Code

Make
Scale from 1 to 100M units
Prototype and Mass- Produce at Same Form Factor
Ecosystem Partners

Chiplet Vendors

Design and SCM

Manufacturing

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Hardware innovation needs quick iteration in chip building
TECHNOLOGY OVERVIEW
Silicon Integration Evolution
(Homogeneous Integration)

Traditional PCB

System on Chip

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Silicon Integration Evolution
(Heterogeneous Integration)

2.5D

SIP/MCM

zGlue integration Platform (ZiP)

Multiple ICs/Dies

Multiple ICs on zGlue

zGlue: Chip + Interposer

Connectivity
CPU + Memory
Power/Analog

Sensors

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zGlue integration Platform (ZiP)
zGlue integration Platform (ZiP)

zGlue Smart Fabric
(Programmable Silicon Chip + Interposer)
zGlue integration Platform (ZiP)
zGlue Smart Fabric

Programmable Routing Fabrics

a) Analog
b) Digital
## Analog Signal Fabric

<table>
<thead>
<tr>
<th>Connection</th>
<th>Switch</th>
<th>Chiplet</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Connection</td>
<td>Switch</td>
<td>Chiplet 1</td>
<td>Processor</td>
</tr>
<tr>
<td>Connection</td>
<td>Switch</td>
<td>Chiplet 2</td>
<td>Memory</td>
</tr>
<tr>
<td>Connection</td>
<td>Switch</td>
<td>Chiplet 3</td>
<td>Radio</td>
</tr>
<tr>
<td>Connection</td>
<td>Switch</td>
<td>Chiplet n</td>
<td>Sensor &amp; Actuator</td>
</tr>
</tbody>
</table>

- **Field Programmable Configuration Bits for Switch Control**
- **Configuration Bus**
- **Configuration Port**
- **Configuration Update Memory Controller**
- **One Time Programmable (OTP) Memory**
- **Non-Volatile RAM (NVRAM)**

Additional components include:
- **Fabric and IO Controller**
- **Self Test**
- **Power Manager**

Diagram featuring interconnections and components labeled with various ports and switches.
zGlue Smart Fabric -> ZiP Chip

Benefits
1. Extend Battery Life
2. BOM Reduction

Benefits
1. Fast Time to Market
2. Path to Quick Iterations

Chiplets
Pre-Fabricated in Production ICs from any Vendor (WLP/CSP/BGA)

Available in
CoB, CoG, QFN, LGA, BGA

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ZiP Packaging Options

CoB/CoG ZiP

QFN/LGA ZiP

BGA ZiP
Smart Fabric Surface IO Interface

(a)

(b)

Cu microbumps on zGlue Surface

Solder balls on Chiplet

Chiplet solder ball makes connection to many zGlue microbumps. Notice the imperfections in the roundedness due to solder reflow to the copper microbumps.
Chicago ZiP Chip

ZiP for Wearables, Fitness, Bio

CortexM4 MCU + BLE
Temperature Sensing
Vibration, Steps (Accel)
Roll and Pitch (Compass)
Battery Recharging
Heart Rate Sensor
Electronic Repair After Assembly

ReAlign Test and Config Block

zGlue Si Interposer Chip

zGlue Surface Bumps

Attached Block Die

Test Pattern Transmit on 8h
Test Pattern Receive on 8i
Test Pattern Receive on 8g
Test Pattern Transmit on 8h

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Dallas ZiP Chip

- Dialog MCU
- mCube Accelerometer
- Macronix Flash
- Maxim Battery Charger
- SiTime RTC
- Analog Devices EKG AFE
- zGlue 7x7
Repair Results
zGlue Integrated Power Management

Processor

Radios

Memory

Sensors

Integrated Voltage Regulators

Vbat
Flexible Power Tree with nanoPower IQ

- Wide Input Voltage Range: 0.8V to 5.5V
- 6x Power Function Blocks
- Flexible Power Routing to Internal and External Components
- nanoPower Quiescent Current IP
Power Shedding—Cut Leakage

Conventional

Full control over power control on the Smart Fabric: Opening up, reactivation and power gate
Design and Application Flow

Chipbuilder.zglue.com
ChipBuilder™ CAD
http://chipbuilder.zglue.com
V2.0 Launched Today at Sensor Expo in San Jose, CA

• Services
  • Cloud based Chip Design
    • Select Components (150 Chiplet
    • Place and Route
    • DFM, DRC, LVS
  • Connected Dev Kits

• Usage
  • System - System design
  • Firmware Coding – SDK/API

Automation drives down AE costs.
ChipBuilder Demo

https://www.youtube.com/watch?v=O7rf6cu6KwQ
Chicago ZiP Chip

ZiP for Wearables, Fitness, Bio

CortexM4 MCU + BLE
Temperature Sensing
Vibration, Steps (Accel)
Roll and Pitch (Compass)
Battery Recharging
Heart Rate Sensor
ZGlue chiplet info Exchange Format (ZEF)

A Machine Readable Chiplet Description

Open Source Input Format

Defines file formats and structure for a) Mechanical, b) IO, c) Electrical, and d) Architectural Attributes

Data arranged in a CSV format with a number of standardized variable names;
For Example Try Reading the following Chiplet

```
x  y  z
1280 1790 520
```

A More Complete Mechanical:
Reference, Part_value, MPN, Order_Number, Container, Pieces_per_unit, Name, Pkg_type, Pkg_IPC_code, SMT_compatible, Width_x, Width_tolerance, Length_y, Length_tolerance, Thickness_z, Thickness_tolerance, Count_IO, Bump_pitch, Bump_pitch_tol, Bump_dia, Bump_dia_tol, Bump_thickness, Bump_thickness_tol, Bump_material, Mold Material, Reflow Profile

More details at https://github.com/zglue/ZEF
zGlue smart fabric is programmable silicon designed to be the base for chip stacking. Developer uses zGlue online software to stack chiplets and build a system on chip stacks. All the software to design, program, and manufacturing the system is made available via an online portal.

**Step 1: Select Components**
Programmable silicon base for stacking. ‘Glue’ chiplets in z direction.

**Step 2: Build, Optimize and Code**
Place, design capture, route, test, download API and SDK, order devkits, order volume

**Step 3: Manufacture**
Shuttle prototype
Ramp up volume. (Hardening option available for HVM)
ECONOMICS OF CHIPLETS
Chips on Organic Substrate

Mature Back End (BE) assembly

Unit BoM Cost (MCM) \( \propto \{p1 \times Area_{C1} + p2 \times Area_{C2} + p3 \times Area_{C3} + p4 \times Area_{C4} \} + \{p6 \times Area_{Substrate}\} + A&T\text{Cost} \)

• Board Modules
• Legacy Multi Chip Modules (MCM)
• System in Package (SIP)
• Cost-Down, Size-Down Value-Add Play
• Can be re-package as QFN, LGA, BGA etc.
Single Chip SoC

Mature, Expensive, Not always possible

Unit BoM Cost (MCM) \( \propto \{p1 \times \text{Area}_C5\} + \{p7 \times \text{Area}_\text{Substrate}\} + \text{A&TCost} \)

- Single Chip Integration
- Large NRE Costs (Only large volumes justify)
- Lowest Unit Costs?
- Best Performance?
- Is it even Possible to Integrate so many functions on one die? Hence Heterogeneous Integration
Active Silicon Interposer CoB

Innovative FE (arch), Innovative BE (Design & assembly)

\[
\text{Unit BoM Cost} \propto (p_1 \times \text{Area}_C1 + p_3 \times \text{Area}_C3) + \{p_5 \times \text{Area}_\text{Si\_Interposer}\} + \{p_8 \times \text{Area}_\text{Substrate}\} + \text{A&TCost}
\]

- This is where interesting economics exits.
- Value of the smartness in Si Interposer needs to justify the cost. AND IT DOES. You just need to know how to design for that.
- The system level NRE and units cost can be lower than implementations while offering TTM and size advantage.
- SLT is complicated.

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zGlue
Active Silicon Interposer LGA/BGA

Innovative FE (arch), Innovative BE (Design & assembly)

Unit BoM Cost $\propto \{p_1 \times \text{Area}_C1 + p_3 \times \text{Area}_C3\}$
+ $\{p_5 \times \text{Area}_{\text{Si Interposer}}\}$
+ $\{p_8 \times \text{Area}_{\text{Substrate}}\} + \text{A&TCost}$

- Added Cost to Re-Package
- Easier to Sell
- Easier to Perform SLT
Summary

- zGlue = Glue Chiplets in z Direction and Make Custom Chips
- zGlue Smart Fabric is a Silicon Active Interposer Chip
- Available Products: Shuttle Prototypes, Dev Kits, Volume Ramp, Hardened ZIP Chips
- Main Portal to Engage with the Company is http://Chipbuilder.zglue.com
- Economically Viable

For more info contact business@zglue.com
OR contact me at jawad@zglue.com
Building New Breed of Chips to Power IoT