THE STRENGTH OF BONDING: THE LETI EXPERTISE ON BONDING
General definition:
Wafer bonding enables to temporarily or permanently join two substrates (processed or not) using an adapted technology.
WAFER BONDING CLASSIFICATION

Wafer Bonding

No Intermediate layer
- Direct bonding
- Anodic bonding

With Intermediate layer
- Conductive layer
- Mixed surface
- Insulating layer
- Direct bonding
- Thermo compression
- Eutetic bonding
- Polymer bonding
- Direct bonding
- Glass frit bonding
- Polymer bonding
Spontaneous bonding without “thick liquid” material.
DIRECT BONDING

Spontaneous bonding without “thick liquid” material.

- Versatile process
- Mass production demonstrated
- µelectronics and µtechnology processes compatibility
- Could be a low temperature process

Critical surface preparations
(roughness, flatness, defect level…)

Surface preparations

Polishing
Wet cleaning
Plasma
Ion beam surface activation

Bonding
DIRECT BONDING

Adhesion energy

\[
U = \frac{(2\gamma)^{5/4}}{\eta t^{3/4}} \left( \frac{E}{1 - \nu^2} \right)^{0/4} \left( \frac{1}{9A^{3/4}} \right).
\]

Adherence energy

(“Bonding energy”)

=> DCB Anhydrous bonding energy is:
more «realistic»
more «discriminating» for mechanism
SI/SiO2 AND SiO2/SiO2 BONDING MECHANISM

Surface conditioning (cleaning, roughness, binding states, etc.)

Room temperature and atmospheric pressure bonding:
Van de Waals adhesion on “rough surface”

Complete direct bonding mechanism with water as key enabler

Bonding states evolution upon annealing: from Van der Waals to covalent bonding

The Smart Cut™ technology: a success story

SOITEC (created in 1992)
Today: more than 1000 people and world’s leading supplier of (SOI) wafers

LETI Smart Cut™ patent: Michel BRUEL
The Smart Cut™ technology => Innovative substrate

« Integrate new materials and functionalities in order to improve devices performances and enlarge application spectrum »

Active layer Eng.
- strained silicon
- Germanium
- GaN
- LiTaO$_3$ / LiNbO$_3$

Applications
- High mobility
- High mobility / hybrid circuits
- RF and LEDs
- RF MEMS / Probe memories

BOX Eng.
- Alternatives BOx
- patterned BOx
- Ultra thin BOx

Thermal issues / ESL
- Mixed circuits
- Multi Vt / Memories

Base Eng.
- HR substrates
- Quartz substrate

RF applications
- Optic applications (imagers, …)

... Etc …
CU/CU BONDING MECHANISM

Surface conditioning (cleaning, roughness, binding states, etc.)

Room temperature and atmospheric pressure bonding:
Van de Waals adhesion on “rough surface” to CuO\(_2\) full oxide bonding

Binding states evolution upon annealing: from oxide bonding to metallic bonding

DIRECT BONDING : HYBRIDE BONDING

- Thanks to Classical Damascene layer => Cu/SiO₂ hybrid surface
- Compatible with direct bonding requirement
- Interconnexion at the bonding interface Pitch => 1-2µm

CuOₓ (~3 nm)

Demixing CuO₂

500nm
DIRECT BONDING : HYBRIDE BONDING

**EVG Gemini**

- Front to Front optical alignment
- Insitu Infra red alignment control => Close loop
- Insitu activation/cleaning surface

- Alignment / bonding wave

Global alignment:
10nm @ 3σ 195 nm

1µm pitch (0,5µm Cu pad)

Red key : Top
Green key : Bottom
New 3D imager sensor development with W2W hybrid bonding

Hybrid bonding interface

Direct hybrid bonding of BEOLs levels

Image Sensor

Image Signal Processor (ISP)

CMP Improvement
Hybrid bonding

Typical Cu/Cu bonding pad with Cu crystal growth during bonding interface disappearance.

Die to wafer:

Alignment and die bonding using SET FC1

Bonding on 200mm or 300mm wafer (yield depend on die size and complexity)

Alignment measurement with EVG AVM <=2µm

DIE TO WAFER DIRECT BONDING FOR PHOTONIC

Die to wafer: More complex to clean & manipulate after dicing

=> yield: 100% bonded die and 80-90% perfect interface

Stop etch layer

Photonic SOI

Die-to-Wafer bonding flow

1. CMP

2. Top die dicing

3. Holder placement

4. Cleaning

5. Die-to-Wafer stacking

http://picmos.intec.ugent.be
DIRECT WAFER BONDING FOR MOORE LAW

SOI Substrates
Mobility booster (sSOI, GeOI, …)
Ultrathin Buried Oxide
Alternatives Buried Oxide (SiNx, C*, …)

Monolithic 3D for further density scaling

P. Batude, VLSI 2011
AND ENABLING MORE THAN MOORE…

**Hermetic Wafer Level Packaging**
S. Nicolas et al, ECTC 2014

**RF Filters**
Piezoelectric thin film transfer
JS Moulet et al, IEDM 2008
B. Imbert, IFCS 2011
Undisclosed industrial partner

**3D Applications**
- High performances RF Filters
- 3D stacked CMOS imager
- Wide I/O Demonstrator
- High density 3D Silicon Interposer

**Dutoit et al., VLSI Circuits 2013**

**J. Charbonnier et al., ESTC 2012, ECTC 2013**

**R Taibi et al, IEDM 2011**
CEA-LETI BONDING ECOSYSTEM

- Fundamental research through **academic collaborations**
  
- **R&D partnership** with
  - Soitec (20 years long collaboration)
  - EV Group (from 2013)
  - ST microelectronics

- Industrial **equipment suppliers** collaboration

- More than **60 patents** related to bonding tech. and app.

- **International recognition** with conference board
  - ECS (Wafer bond symposium), WaferBond Conference
KEY MESSAGES

- Wafer bonding is not just a technique…
- It is also a properties enabler
- Leti has pioneered wafer bonding for the microelectronics 20 years ago with the SOI technology and will continue to master wafer bonding expertise with a State-of-the-art equipment set and building collaborative work with key players
Thank you for your attention