OUTLINE

• Introduction to Soitec

• Soitec & CEA Leti: a strong & long-term innovation & development partnership

• Presentation of the Substrate Innovation Center

• Substrate Innovation Center: enabling exploring solutions & material integration
Soitec – Who we are

We design and deliver innovative substrates & solutions to enable our customers’ products shaping everyday life.

DESIGNER & MANUFACTURER OF INNOVATIVE SEMICONDUCTOR MATERIALS

1450 Employees Worldwide

GLOBAL PRESENCE

4 Core Technologies
SMART CUT, SMART STACKING, EPITAXY

3 High-growth Markets
SMARTPHONES, AUTOMOTIVE, CLOUD INFRASTRUCTURE, IOT

6 Wafer fabs
300-mm – France (Bernin II) + Singapore*
200-mm – France (Bernin I) + China (via Simgui)
150 mm – France (Bernin III)
150 – 200-mm GaN Epitaxial wafers – Belgium (EpiGaN) CAPABILITY

1 Largest manufacturer of engineered substrates
LEADER

*Production site now qualified by several customers
Soitec’s full range of engineered substrates across multiple segments and applications

**RF Front-End Module**
- RF-SOI
  - For high efficient mobile communication

**Power**
- Power-SOI
  - For seamless high voltage device isolation

**Processor & connectivity SoC**
- FD-SOI
  - For power-efficient & flexible digital computing with easy analog/RF integration

**Piezo on insulator**
- POI
  - New engineered substrates for filters

**Photonics**
- Photonics-SOI
  - To integrate high performance photonics devices into silicon

**Imagers**
- Imager-SOI
  - For improved imager performance in NIR
A global multi-site industrial footprint

- **Bernin 2**
  - RF-SOI
  - Photonics-SOI
  - Power-SOI
  - Total 300-mm capacity → 0.9 M wafers/y. by FY’20
  - Soitec Bernin 1, France - HVM
    - 950K wafers/y. capacity

- **Bernin 1**
  - Total 200-mm capacity → 1.3 M wafers/y. by FY’20
  - Simgui

- **Bernin 3**
  - Total 150-mm capacity → potential of 0.4M wafers/y
  - EpiGaN Hasselt, Belgium

- **Pasir Ris**
  - RF-SOI
  - Power-SOI
  - Planned capacity: 1M wafers/y.
  - Simgui, China - HVM
    - 180K wafers/y. capacity going to 360K wafers/y.

- **Simgui**
  - Power-SOI
  - Other SOI Products
  - Total 300-mm capacity → 0.9 M wafers/y.

- **Soitec Bernin 3**, France - Ready HVM
  - 15K wafers/y. capacity with plan to extend to 400K

- **Soitec Bernin 2**, France – HVM
  - 650K wafers/y. capacity with plan to extend to 1M

- **EpiGaN Hasselt**, Belgium
  - GAN epitaxial wafer

- **Pasir Ris**, Singapore - HVM
  - Planned capacity: 1M wafers/y.
Smart cut™ technology at the heart of innovation

**TECHNOLOGY**

- Industrial manufacturability of SOI – high yield
- Drastical improvement of uniformity & quality
- Re-use of donor wafer provides optimum cost efficiency
- Flexibility of material integration

1. Initial silicon
2. Oxidation
3. Implantation
4. Cleaning and bonding
5. Splitting
6. Annealing and CMP touch polishing
7. Donor wafer becomes new wafer A

SOI wafer

**Base wafer = mechanical support**
**Silicon or easy to handle & active**

**Active layer**

**Functional/insulator layer**
A long and fruitful innovation and development collaboration since the 90’s, accompanying the Soitec’s growth
Soitec & CEA-Leti: a strong & long-term innovation & development partnership

Oriented Single-Crystal LiTaO$_3$ Thin Film on Silicon for High Performances SAW Components

Full InGaN based LED: towards a native full-color micro-display solution

SiGe nano-heteroepitaxy on Si and SiGe nano-pillars

Beyond advanced FDSOI: Low Temp SmartCut for enabling High Density 3D SoC applications

In 2018, 13 publications issued from CEA & Soitec collaboration
Soitec & CEA-Leti: a strong & long-term innovation & development partnership

In the top 50 of French patent applicants INPI ranking over the past 2 years

- N°1 of the French mid-size companies for patent filings
- >3500 patent applications

CEA: in top 4 of French patent applicants

- CEA-LETI: n°1 of the microelectronic R&D Institute in Europe
- 2760 patents in portfolio

In 2018, 12 patents filed from CEA & Soitec collaboration

CEA & SOITEC: a shared culture and mindset for Innovation
Expanding the collaboration: the Substrate Innovation Center

- Expanding SOITEC’s R&D depth while keeping compatibility with internal R&D corridors
- Accessing new ideas, disruptive process improvements, larger expertise
- Early prototyping, focus on lead time and quality
From innovation to high quality prototyping

Engineered substrate development capabilities enlarged to non-standard process steps
Compatible with high level of expectation: Quality, Cost & Cycle Time

- Expertise
- Infrastructure
- Flexibility
- Network

- Expertise
- Development
- Industrialization know-how
- Network

Up to 730+ tools
10,000m² cleanroom

10 Soitec assignees
@ Leti (today)

18 programs
>10 materials
6 application fields
Full 200 & 300mm SOI process line available at CEA-Leti (state of the art manufacturing equipments for advanced substrates)

Specific SOITEC’s equipment hosted in ultra front-end cleanroom area at CEA-Leti

Methodology sharing and fast learning cycles between joint teams

Recurring lots started to support prototyping & innovation
From innovation to high quality prototyping, examples

**Layer deposition tool matching**

- **Phase 1**: Identify characterization solutions (Leti equipment)
- **Phase 2**: Define conditions of characterization tool utilization & train Soitec assignee
- **Phase 3**: Soitec autonomous to perform its own characterizations

**CMP process development**

- **Phase 1**: 1st development at CEA-Leti
- **Phase 2**: 1st prototyping (mix Soitec / CEA-Leti resources)
- **Phase 3**: Soitec process implementation

**200mm prototype (non standard materials)**

- **Phase 1**: R&D - 1st pipe cleaner
- **Phase 2**: Full process CEA-Leti
- **Phase 3**: Production ramp up

**In-progress**

- Prototyping Mix flow Soitec / CEA-Leti
Substrate innovation center: an enabler for exploratory solutions

Improved processes

ENGINEERED SUBSTRATES
Anything on anything

New materials

SMART CUT™

New structures

SCOTTING STACKING™

New segments

EPITAXY

Device Layer:
- Silicon, Strained Silicon, Germanium, III-V...

Buried Insulator: SiO2, ONO...

Handle Substrate:
- CZ Silicon, High-resistivity Si, Sapphire, Glass

Capital market day, Soitec, 13th of June 2019
Substrate innovation center: an enabler to new products & applications, recent examples

SOI with cavities

Single-crystal layer stacking

Piezoelectric

InGaNOS

MEMS cMUT

3D monolithic integration

RF filters

µLEDs
Substrate innovation center: a new hub for strong collaborative innovation

- From years, Soitec and CEA are strongly engaged together in large scale collaborative programs

Enlarge partnerships with key actors across the entire supply chain
Substrate innovation center: take-aways

Substrate Innovation Center: the next era of the CEA-Soitec collaboration with:
- An intimate link between pilot line and industrial mass production
- Direct validation of concepts, from materials to devices
- Integrate major actors to increase the capabilities for advanced substrates development and prototyping
As strategic components for microelectronics, Soitec’s technologies and CEA-LETI (FD-SOI, RF-SOI, POI, Photonics-SOI and InGaNOS) are supported by Nano 2022 – the French leg of the IPCEI program, aiming to strengthen Europe's ecosystem and ensure industry growth.

Europe is involved in the Région Auvergne Rhône-Alpes through Soitec’s equipment inside the Substrate Innovation Center